IN THE CLAIMS

1. (Original) A method for forming a via in an integrated circuit packaging substrate comprising:

making a via opening having a base, the base of the via opening positioned at a selected level that includes conductive material within the integrated circuit packaging substrate;

depositing an interfacial layer material within at the base of opening;

placing a conductive material over the interfacial material; and

heating the materials at the base of the opening.

2. (Original) The method for forming a via of claim 1 further comprising masking the surface of the integrated circuit packaging substrate, a mask being formed having a mask opening therein positioned above to the base of the via opening.

3. (Original) The method for forming a via of claim 3 wherein depositing an interfacial layer material within the via opening includes sputtering the interfacial material onto the mask and into the via opening; and

wherein the method further comprises removing the mask.

4. (Original) The method for forming a via of claim 1 wherein interfacial layer material is a material that will diffuse into the conductive material at the temperature produced by heating the materials at the base of the via opening.

5. (Original) The method for forming a via of claim 1 wherein the interfacial material is selected from the group consisting of palladium, platinum, cobalt or nickel.

6. (Original) The method for forming a via of claim 1 wherein the interfacial material includes palladium.

7. (Original) The method for forming a via of claim 1 wherein heating materials at the base of the via opening includes directing energy from a laser at the base of the opening.

8. (Original) The method for forming a via of claim 7 wherein the laser energy is higher at the center of the laser.

9. (Original) The method for forming a via of claim 7 wherein the laser produces temperatures at the base of the via opening in the range of 400 to 600 degrees C.

10. (Original) The method for forming a via of claim 7 wherein the laser has a diameter of approximately half the diameter of the base of the via opening.

11. (Original) The method for forming a via of claim 1 wherein placing a conductive material over the interfacial material includes plating copper within the via opening.

12. (Original) The method for forming a via of claim 1 wherein placing a conductive material over the interfacial material further comprises:

plating electroless copper at the base of the via opening; and

plating the via opening with electrolytic copper.

13. (Original) The method for forming a via of claim 1 further comprising capping the via.

14. - 20. (Canceled)

21. (Original) A method for forming a via in an integrated circuit package substrate comprising:

embedding an interfacial adhesion layer at a base of a via; and

heating at least the interfacial adhesion layer.

22. (Original) The method of claim 21 wherein embedding the interfacial adhesion layer further includes placing a conductive material over the interfacial adhesion layer.

23. (Original) The method of claim 21 wherein heating the materials at the base of the via includes directing the energy of a laser at the base of the via.

24. (Original) The method of claim 21 wherein heating the materials at the base of the via includes heating the materials at the base of the via to a temperature within the range of 400-600 degrees C.

25. (Original) The method of claim 21 wherein the interfacial adhesion material interdiffuses with the conductive material.

26. (Original) The method of claim 25 wherein the interdiffusion of the interfacial adhesion material and the conductive material is nonuniform.

27. (Original) The method of claim 25 wherein the interdiffusion of the interfacial adhesion material and the conductive material forms teeth-like structures that extend into the conductive layers at the base of the via.

28. - 30. (Canceled)

31. (New) A method for forming a via in an integrated circuit package substrate comprising:
placing an interfacial adhesion layer at a base of a via;
placing a conductive material over the interfacial adhesion layer; and
stitching the interfacial adhesion layer and the conductive material.

32. (New) The method of claim 31 wherein stitching the interfacial adhesion layer and the conductive material includes forming a solution of the interfacial adhesion layer and the conductive material.

33. (New) The method of claim 31 wherein stitching the interfacial adhesion layer and the conductive material includes forming a plurality of structures of the interfacial adhesion layer and the conductive material.

34. (New) The method of claim 31 wherein stitching the interfacial adhesion material and the conductive material includes forming teeth-like structures that extend into the conductive layers at the base of the via.

35. (New) The method of claim 31 wherein stitching the interfacial adhesion layer and the conductive material includes heating the materials at the base of the via.

36. (New) The method of claim 35 wherein heating the materials at the base of the via includes heating the materials at the base of the via to a temperature within the range of 400-600 degrees C.

37. (New) The method of claim 35 wherein heating the materials at the base of the via includes directing a laser at the base of the via.

38. (New) A method for forming a via in an integrated circuit package substrate comprising:

placing an interfacial adhesion layer at a base of a via;

placing a conductive material over the interfacial adhesion layer; and

interdiffusing the interfacial adhesion layer and the conductive material.

39. (New) The method of claim 31 wherein interdiffusing the interfacial adhesion layer and the conductive material includes forming a plurality of structures of the interfacial adhesion layer and the conductive material.

40. (New) The method of claim 31 wherein interdiffusing the interfacial adhesion layer and the conductive material is achieved by heating the materials at the base of the via.